REMARKS

I. THE ANTICIPATION REJECTION

Claims 1, 3, 5, 7-9, 11, 13 and 15 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. patent 5,870,289 to Tokuda et al. Claims 1 and 9 are independent, and the remaining claims are dependent, either directly or indirectly, on one or other of claim 1 or claim 9. The rejection is respectfully traversed.

Claim 1 is directed to a microelectronic package comprising a first level substrate including a plurality of microelectronic devices and a plurality of first level substrate input/output pads in a face thereof. A thin film decal is provided on the face of the first level substrate, the thin film decal including first and second opposing faces, a plurality of first decal input/output pads on the first face, at least one of which is electrically connected to at least one of the first level substrate input/output pads. A plurality of second decal input/output pads is provided on the second face and at least one internal wiring layer that is electrically connected to at least one of the first and second decal input/output pads. A second level substrate is provided which includes a plurality of second level substrate input/output pads on a face thereof, and a dielectric adhesive layer is adhesively bonded to the thin film decal and to the second level substrate. The dielectric adhesive layer includes a plurality of conductive vias therein that electrically connect at least one of the second level substrate input/output pads to at least one of the second decal input/output pads.

The Examiner refers to Figure 6 of Tokuda in support of the anticipation rejection of claim 1. However, it is unclear which features of Figure 6 of Tokuda the Examiner is seeking to map to the terms of the claim. In applicant's view, there are only two relevant interpretations, neither of which is believed to give rise to anticipation of the claims of this case.

Figure 6 of Tokuda shows a multi-level chip package with a number of layers. The most relevant layer for present purposes is the one labelled 451-n, which is the lowest chip-carrying layer in the figure. However, the reference numerals for the component parts of the layer are only given in the case of the uppermost layer. In the following discussion, reference will be made to those reference numerals with the understanding that the references should be transcribed to layer 451-n.

If the first level substrate in the claim is equated with adhesive film 430, then the input/output pads arguably map to the top of the through-hole connections 440. The substrate 420 can then be mapped to the thin film decal, the second level substrate mapped to the package base 480, and the dielectric adhesive layer mapped to the adhesive film 462 (as suggested by the Examiner). However, this falls a long way from anticipating the claims.

First, the thin film decal (substrate 420) has no first decal input/output pads on the first face, because the through-hole connections 440 pass all of the way through the adhesive film 430 and the substrate 420. Secondly, the second level substrate (package base 480) does have input/output pads (I/O pins 490) but these do not electrically connect to the dielectric adhesive layer, as specified in the last four lines of

claim 1. Thirdly, the adhesive film 462 has no plurality of conductive vias, as specified in the penultimate line of claim 1.

If a different interpretation is taken, in which the adhesive film 430 and substrate 420 are considered together to comprise the thin film decal (which then arguably has input/output pads on the first and second faces), then there is no first level substrate as required by claim 1.

In light of the above, it is clear that claim 1 is not anticipated by Tokuda. Withdrawal of the anticipation rejection of that claim and all claims dependent thereon is accordingly respectfully requested.

Referring to claim 9 (the second independent claim in the case), the Examiner seeks to map the chip carrier 451-n onto both the substrate and the decal of claim 1. In respect of the dielectric adhesive layer, the same point as made above in respect of claim 1 applies to the lack of conductive vias. Furthermore, the Examiner seeks to map the "release layer" in the claim onto the adhesive film 461-n. Reference to Figure 5 of the present application together with the accompanying description will illustrate the purpose of the release layer 212. This layer may be removed, for example by laser irradiation, to allow the decal to be freed from the substrate. There is absolutely no teaching or suggestion in Tokuda that adhesive film 461-n is capable of performing such a release function. Moreover, attempting to remove this layer would simply destroy the multi-chip module 400 shown in Figure 6.

It is clear that claim 9 is not anticipated by Tokuda. Withdrawal of the anticipation rejection of that claim and all claims dependent thereon is accordingly respectfully requested.

II. THE OBVIOUSNESS REJECTIONS

Claims 2, 4, 10 and 12 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Tokuda in view of U.S. Patent 5,640,051 to Tomura et al. Claims 6 and 14 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Tokuda in view of U.S. Patent 5,121,229 to Frankeny et al. Those rejections are respectfully traversed.

The claims rejected on obviousness grounds are dependent either directly or indirectly on claim 1 or claim 9. Tokuda is irrelevant so far as claims 1 and 9 are concerned, for the reasons discussed above. The deficiencies are not cured by Tomura or Frankeny, and a person of ordinary skill would not have been motivated to resort to those disclosures in the context of the present invention. The combined disclosures of Tokuda with Tomura or with Frankeny do not give rise to a *prima facie* case of obviousness. Withdrawal of the outstanding obviousness rejections is accordingly respectfully requested.

Allowance of the application is awaited.

Respectfully submitted,

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